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Plasma-optimized contact for high-performance PdSe₂ nanoflake-based field-effect transistors

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ABSTRACT

Low-resistance contact has long been pursued in the two-dimensional (2D) electronic/optoelectronic device community. Still, an economy-efficient method highly compatible with the conventional 2D device fabrication process in laboratory remains to be explored. Herein, we report a plasma-optimized contact strategy for high-performance PdSe₂ nanoflake-based field-effect transistors (FETs). Selenium vacancies created by air plasma can introduce *p*-type doping in the contact area, thus optimizing the device performance. The effect of plasma treatment on PdSe₂ nanoflake is corroborated by high-resolution transmission electron microscopy, energy-dispersive x-ray spectroscopy spectrum, atomic force microscopy, and Kelvin probe force microscopy. The PdSe₂ FET with plasma-optimized contact exhibits significantly improved field-effect carrier mobilities, current on/off ratios, and reduced contact resistance than that without plasma treatment fabricated from the same PdSe₂ nanoflake. Moreover, this strategy has also been proven effective to prepare high-performance FETs based on 2D WSe₂ and MoSe₂ nanoflakes, further demonstrating its application prospect.

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Two-dimensional (2D) van der Waals (vdW) materials provide a promising platform for constructing advanced electronics/optoelectronics in this post-Moore era,[1–9] where the silicon (Si) technology is approaching its physical limit.[10,11] However, electrical contact remains challenging for 2D devices, severely impeding their step into commercial products.[12–14] Recently, researchers have developed different strategies to tackle the electrical contact issue.[15–29] These methods cover the application of the edge-contact geometry instead of the conventional surface-contact geometry,[15–17] the creation of the vdW contact [e.g., via transferred metal electrodes,[18,19] usage of low-melting-point metal,[20] insertion of atomically thin 2D materials, such as hexagonal boron nitride (h-BN)[21] and graphene,[22] deposition of selenium (Se) as the buffer layer[23]], the introduction of the semi-metallic elements to

fill in the gap states,[24,25] inducing phase transition between semiconducting and metallic phases to reduce contact resistance,[26] and the improvement of the contact in a molecule optimization strategy.[27] These works significantly alleviated the contact issue, but with the price of heavy fabrication burden and high cost, thus limiting their application prospect. At the time of writing, a contact optimization strategy with high economic efficiency and compatibility with standard 2D device fabrication processes in laboratories is still urgently wanted.

Palladium diselenide (PdSe₂) is a 2D noble metal dichalcogenide with the thickness-dependent bandgap.[30–33] Its bandgap reduces from ∼1.4 eV in the monolayer limit to <0.5 eV in bulk.[31,33] The tunable bandgap and high air stability enable it to be applied in various

devices, especially as high-performance infrared photodetectors in mid-wave infrared to long-wave infrared regimes.[32–35] Plasma treatment is a widely used method to synthesize 2D materials and modify their physical/chemical properties.[36] There are already some works involving leveraging plasma treatment to reduce PdSe$_2$ thickness for better electrical performance,[37,38] but they focused on the morphology modification of PdSe$_2$ rather than the contact improvement. Moreover, introducing plasma in their experiments considerably increases the device fabrication complexity. In this regard, a contact optimization strategy highly compatible with the conventional 2D device fabrication process is rarely reported.

In this Letter, we present a simple but effective plasma-optimized contact strategy for PdSe$_2$ nanoflake-based field-effect transistors (FETs). Our method shows high compatibility with the standard fabrication process of 2D devices in laboratories. Before the electrode deposition, we only need to place the samples, the contact areas are exposed by electron beam lithography, in the basic plasma cleaner for plasma treatment. Compared with the PdSe$_2$ FETs without plasma-optimized contact fabricated from the same nanoflake, the treated counterpart exhibits a ∼2.6-fold increase in field-effect carrier mobilities, a ∼2.3-fold increase in the current on/off ratio, and a ∼2.7-fold decrease in the contact resistance. The high-resolution transmission electron microscopy (HRTEM) result indicates a crystalline–amorphous phase transition induced by the plasma treatment, and the plasma-induced p-type doping was confirmed by the Kelvin probe force microscopy (KPFM). More interestingly, we observed a transition between n-type and p-type dominated transport behaviors with decreasing the temperature. In addition to PdSe$_2$, our contact strategy can be further extended to WSe$_2$ and MoSe$_2$ FETs, demonstrating its broad application prospect.

Figure 1 compares the conventional evaporated contacts and the plasma-optimized contact strategy, where the only difference lies in the plasma treatment on the contact areas before the electrode deposition, requiring no other additional process and thus highly compatible with the standard 2D device fabrication process in laboratories. To confirm the effectiveness of this contact optimization strategy, we prepared a pair of devices with/without plasma treatment from the same PdSe$_2$ nanoflake as shown in the supplementary material Fig. S1. Starting from the mechanically exfoliated PdSe$_2$ nanoflake on the silicon dioxide/silicon (SiO$_2$/Si, SiO$_2$: 300 nm) substrate [step 1 in the supplementary material Fig. S1(a)], the contact areas of PdSe$_2$ FET were first exposed by the standard EBL [step 2 in the supplementary material Fig. S1(a)], followed by the air plasma treatment on the contact areas in a basic plasma cleaner (Harrick Plasma, PDC-32G-2) at a pressure of ∼0.74 Torr for 5 min at radio frequency (RF) power of 18 W [step 3 in the supplementary material Figs. S1(a) and S2]. The other part of the PdSe$_2$ nanoflake was protected from the plasma treatment by poly(methyl methacrylate) (PMMA), and then, the PdSe$_2$ FET without plasma-optimized contact was defined by the standard EBL again [step 4 in the supplementary material Fig. S1(a)]. The supplementary material Figs. S1(b) and S1(c) provide the schematic illustration of the experimental setup and the optical microscopy image of the fabricated devices, where the electrode metal was deposited by the thermal evaporation of chromium/gold (Cr/Au: 8/60 nm). The thickness of the exfoliated PdSe$_2$ nanoflake is ∼98 nm (supplementary material Fig. S3).

We further measured the basic electrical transport characteristics of the fabricated PdSe$_2$ FETs at room temperature as shown in Fig. 2.
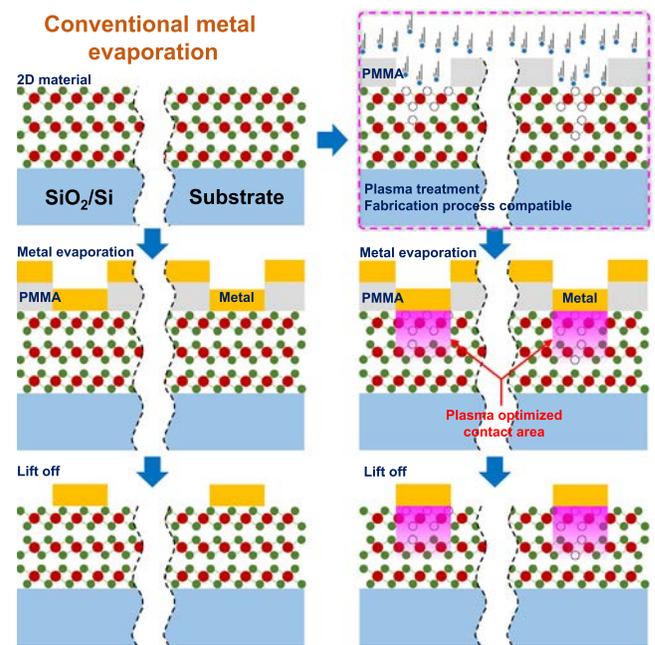
FIG. 1. Schematic illustration depicts the conventional evaporated contacts and the plasma-optimized contact strategy.

Both PdSe$_2$ FETs with/without plasma treatment exhibit n-type dominated ambipolar transport behaviors [Figs. 2(a) and 2(c)]. These ambipolar behaviors are commonly observed in narrow bandgap semiconductors as the thermal excitation at room temperature is sufficient to generate considerable holes/electrons at the valence/conduction band.[39–41] In addition, the much larger current density observed in the PdSe$_2$ FET with plasma-optimized contact [Figs. 2(a) and 2(b)] than its counterpart [Figs. 2(c) and 2(d)] without plasma treatment indicates a much higher carrier injection efficiency enabled by our contact optimization strategy. Meanwhile, the nearly linear curves shown in both output curves suggest the Schottky barriers between the electrode metal (Cr/Au) and the channel in these two devices are small. The current on/off ratios under different back-gate voltages are extracted from their transfer curves [Fig. 2(e)]. Both devices' current on/off ratios in forward/backward sweeping directions increase with the back-gate voltage. For PdSe$_2$ FETs with/without plasma treatment, the maximum current on/off ratios are 18.6/19.5 and 8.5/8.2 at $V_{bg} = 60$ V in forward/backward sweeping directions, respectively.

Meanwhile, the field-effect carrier mobilities are calculated by

$$\mu_{FE} = \frac{g_m}{C_g V_{ds}} \frac{L}{W}, \tag{1}$$

where g_m is the transconductance obtained from the I_{ds}–V_{bg} characteristics, C_g is the capacitance of the 300-nm SiO$_2$ dielectric ($C_g = \varepsilon_0 \varepsilon / d = 11.5$ nF cm^{-2}), V_{ds} is the electrical bias, and L/W is the ratio between channel length and width, respectively. The field-effect carrier mobilities vs back-gate voltage for both PdSe$_2$ FETs in forward/backward sweeping directions are provided in Fig. 2(f), where in both sweeping directions, the maximum field-effect carrier mobilities in PdSe$_2$ FET with/without plasma-optimized contact are
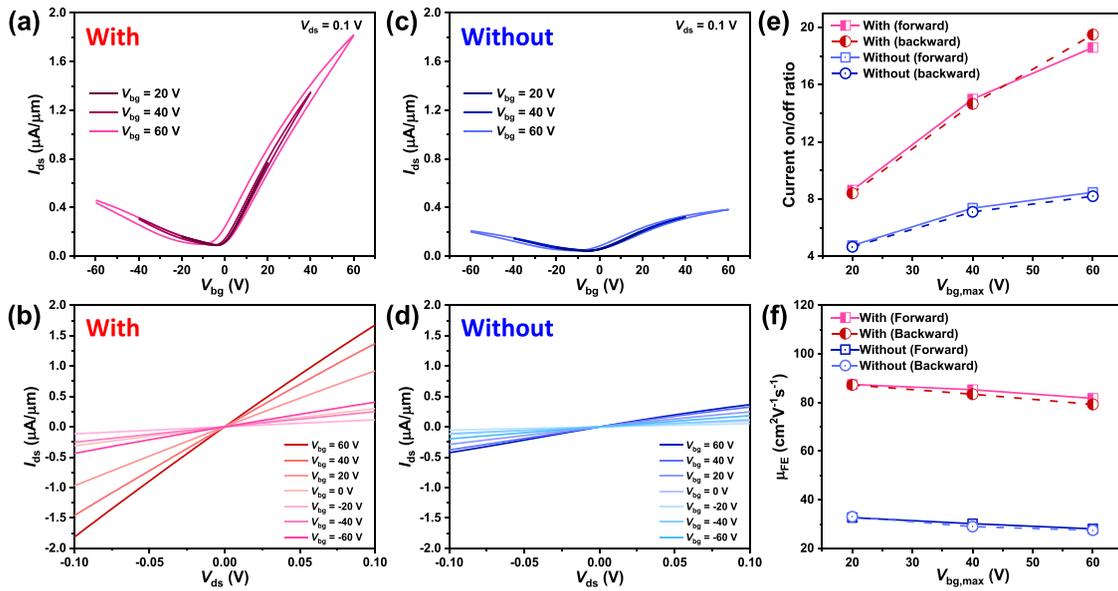
FIG. 2. Electrical transport characterization of PdSe$_2$ FETs with/without plasma-optimized contact. (a) Transfer and (b) output curves in PdSe$_2$ FET with plasma-optimized contact. (c) Transfer and (d) output curves in PdSe$_2$ FET without plasma-optimized contact. Comparison of the (e) current on/off ratios and (f) electron mobilities vs back-gate voltage in PdSe$_2$ FETs with/without plasma-optimized contact.

$\mu_{FE} = 87$ and $\mu_{FE} = 33 \, \mathrm{cm^2 V^{-1} s^{-1}}$, respectively. The superiority of our plasma-optimized contact strategy is emphasized by comparing our device performance with other reports (supplementary material Table S1).

To investigate the contact resistance reduction in the plasma-optimized contact strategy, we applied the transmission line method (TLM) to compare the contact resistance difference in PdSe$_2$ FETs with/without plasma-optimized contact.[42] The rectangular exfoliated PdSe$_2$ nanoflake is extremely suitable to conduct the TLM measurement without additional shaping by the etching treatment. The optical microscopy image of the fabricated devices with variable channel lengths is given in Fig. 3(a), and the fabrication process is the same as that demonstrated in the supplementary material Fig. S1. The electrical contact denoted by red dashed lines was optimized by plasma, while the electrodes denoted by blue dashed lines were without plasma optimization. As indicated by the total resistance vs channel length in Fig. 3(b), for the contact without plasma optimization, the contact

FIG. 3. (a) Optical microscopy image of the device fabricated for contact resistance extractions via the TLM method. (b) Contact resistance extractions of the contacts with/without plasma treatment.

resistance is estimated to be $2R_C = 194 \, \mathrm{k\Omega \, \mu m}$ by its y-axis intercept. On the other hand, for the contact with plasma optimization, the contact resistance decreased to $2R_C = 72 \, \mathrm{k\Omega \, \mu m}$. The significantly reduced contact resistance observed in the plasma-optimized contact strategy can be ascribed to the heavy p-type doping induced by plasma treatment on the contact area, which will be further characterized by KPFM as discussed below.

We also studied the electrical performances of PdSe$_2$ FET by applying plasma treatment on the entire surface of the PdSe$_2$ nanoflake (supplementary material Figs. S4 and S5). To eliminate the experimental factors induced by different nanoflakes, we prepared a pair of FETs on the same PdSe$_2$ sample with only half surface treated by plasma. The device fabrication is summarized in the supplementary material Fig. S4. We first exposed the surface to be treated by plasma by EBL of the mechanically exfoliated PdSe$_2$ nanoflake. The plasma conditions were controlled to be the same as before (5 min at the pressure of $\sim$0.74 Torr). Later, the sample was immersed in acetone for 2 h to remove PMMA, and the paired FETs based on different halves of the same PdSe$_2$ sample were finally defined by EBL, followed by the thermal evaporation of Cr/Au (8/60 nm) electrodes. The room-temperature electrical performances of these devices are given in the supplementary material Fig. S5. Similar to the results obtained in PdSe$_2$ FET without plasma-optimized contact, the PdSe$_2$ FET based on the half without plasma treatment presents n-type dominated ambipolar transport behaviors [supplementary material Fig. S5(a)]. Also, its output curves confirm the small Schottky barrier between Cr/Au and PdSe$_2$ nanoflake again [supplementary material Fig. S5(b)]. In stark contrast, the PdSe$_2$ FET based on the half with plasma treatment exhibits a $\sim$200-fold increase in the on-state current under the same electrical bias [supplementary material Fig. S5(c)]; however, its back-gate tunability is lost. At the same time, the almost linear curves under
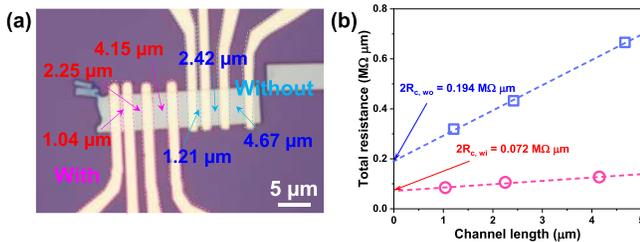
different back-gate voltages presented in its I_{ds}–V_{ds} characteristic suggest the plasma-induced heavy doping on the PdSe$_2$ nanoflake [supplementary material Fig. S5(d)].

The plasma treatment also induced the structural change of PdSe$_2$ nanoflakes, which was identified by scanning transmission electron microscopy (STEM), HRTEM, and atomic force microscopy (AFM). The results are given in Fig. 4. The plasma treatment conditions remain unchanged. As revealed by the STEM image, the PdSe$_2$ nanoflake without plasma treatment preserves the flat surfaces [Fig. 4(a)], while many pinholes appeared on the surface of the plasma-treated PdSe$_2$ nanoflake [Fig. 4(c)]. The typical size of the pinholes is in the range of 10–30 nm. The separated pinholes were assembled into large-area voids when the density of pinholes is high. HRTEM is further used to analyze the plasma-induced phase transition in PdSe$_2$. Figure 4(b) provides the HRTEM image of the PdSe$_2$ nanoflake without plasma treatment, where the sharp lattice fringe confirms its single-crystalline nature. The crystal orientation ([200] and [020]) is indicated by the orthogonal arrows, and the lattice constants along each orientation are $a = 0.28$ and $b = 0.29$ nm, respectively, which are consistent with the previous report.[43] Moreover, the inset provides a fast Fourier transformation (FFT) image of the (002) plane, proving the high quality of the PdSe$_2$ sample. On the other hand, the long-range disordered atomic structure presented in the HRTEM image of the plasma-treated PdSe$_2$ nanoflake [Fig. 4(d)] and the diffuse ring in its FFT image confirm the phase transition from crystalline to amorphous induced by plasma. The phase transition is believed to be resulted by the plasma-induced Se vacancies as suggested by the energy-dispersive x-ray spectroscopy (EDS) spectrum (supplementary material Fig. S6), where the atomic ratio of Se decreased from 65.84% to 48.27% after treatment. We also measured the Raman shift in the PdSe$_2$ samples with/without plasma treatment, as shown in supplementary material Fig. S7. This control experiment was conducted in the same PdSe$_2$ nanoflake as well [supplementary material Fig. S7(a)], and there is no new peak in the plasma-treated half flake

[supplementary material Fig. S7(b)], which suggests the lack of new crystal structure formation and is consistent with the HRTEM results.

Our plasma treatment will also reduce the PdSe$_2$ thickness and induce p-type doping as indicated by AFM and KPFM measurements [Figs. 4(e) and 4(f)]. Before the measurements, we prepared a PdSe$_2$ sample where the areas with/without plasma treatment are distributed alternately, and the plasma conditions were the same as those used in previous experiments. The top panel in Fig. 4(f) illustrates the height profiles obtained along the pink dashed line in AFM mapping given by Fig. 4(e), where the height difference demonstrates that PdSe$_2$ thickness was reduced by ~7.5 nm in the plasma treatment. The surface potential profile across the PdSe$_2$ surface with/without plasma treatment is provided by the bottom panel in Fig. 4(f) along the blue dashed line in the KPFM mapping given in Fig. 4(e). Based on the surface potential difference, the work function difference for PdSe$_2$ nanoflake with/without plasma treatment can be inferred by the following formula:

$$\phi_{with}^{CPD} = \frac{\phi_{tip} - \phi_{with}}{-e}, \tag{2}$$

$$\phi_{without}^{CPD} = \frac{\phi_{tip} - \phi_{without}}{-e}, \tag{3}$$

where ϕ_{with}^{CPD}, $\phi_{without}^{CPD}$, ϕ_{with}, $\phi_{without}$, ϕ_{tip}, and e are the contact potential difference (CPD) between the KPFM tip and the PdSe$_2$ sample with/without plasma treatment, work functions of the PdSe$_2$ sample with/without plasma treatment, KPFM tip, and elementary charge, respectively. Then, the work function difference between the PdSe$_2$ sample with/without plasma treatment can be calculated by rearranging Eqs. (2) and (3),

$$\phi_{without} - \phi_{with} = e(\phi_{without}^{CPD} - \phi_{with}^{CPD}). \tag{4}$$

Based on the bottom panel in Fig. 4(f), it can be concluded that the surface potential of the PdSe$_2$ with plasma treatment is ~100 mV higher than that without plasma treatment; thus, the work function of PdSe$_2$ with plasma treatment is ~0.1 eV larger than that without
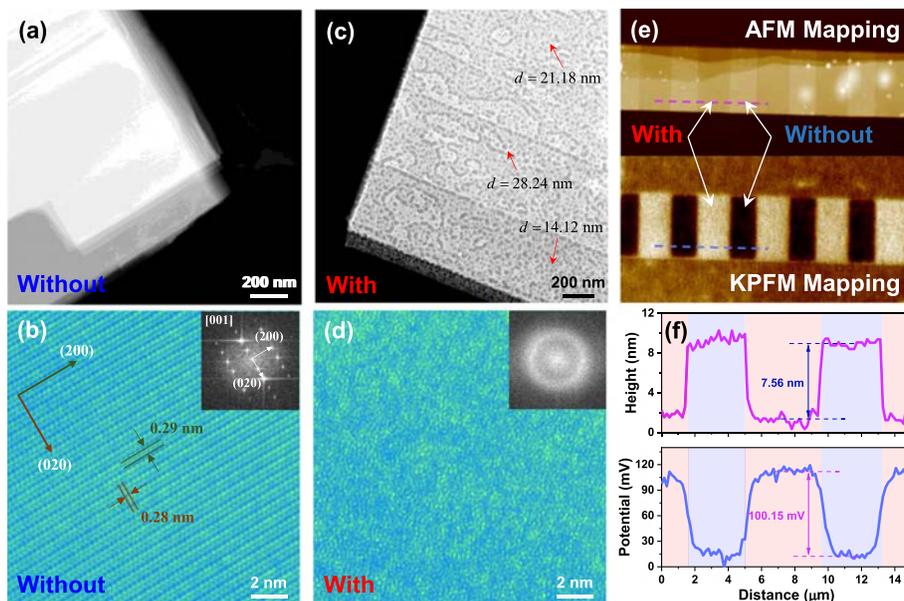
FIG. 4. (a) STEM and (b) HRTEM images of PdSe$_2$ nanoflake without plasma treatment. (c) STEM and (d) HRTEM images of PdSe$_2$ nanoflake with plasma treatment. The insets in HRTEM images show diffractograms obtained by the fast Fourier transform (FFT) of HRTEM images. (e) AFM mapping (up panel) and KPFM mapping (bottom panel) images of the PdSe$_2$ nanoflake partially treated by plasma. (f) Height profile (up panel) and surface potential profile (bottom panel) obtained along the pink line and blue line in (e).

plasma treatment. This observation indicates the plasma-induced heavy p-type doping in the PdSe₂ sample, thus significantly increasing the carrier injection efficiency in this geometry.

To study the plasma-optimized contact's effect on the Schottky barrier height, we continued the low-temperature electrical transport characterization of PdSe₂ FET with/without plasma-optimized contact (Fig. 5). As indicated by the inset in Fig. 5(a), we prepared a pair of PdSe₂ FETs in the same way as introduced before and characterized the middle FET with asymmetric contact (source electrical contact without plasma optimization while the drain contact with plasma optimization). In the measurement, it is interesting to find that as the temperature decreased, a transition between n-type and p-type dominated transport behaviors happened (supplementary material Fig. S8). This phenomenon should be ascribed to the inhibited thermal excitation of electrons at low temperature. In the case of $V_{ds} = 1$ V/$V_{ds} = -1$ V, the contact with/without plasma optimization limits the hole transport [Fig. 5(c)]. The $I_{ds}-V_{ds}$ curves measured at $V_{ds} = 1$ V [Fig. 5(a)] present a larger on-state current than that obtained at $V_{ds} = -1$ V [Fig. 5(b)], demonstrating that plasma-induced heavy p-type doping at the drain electrode will increase the hole inject efficiency. Then, the Schottky barrier heights at the contacts with/without plasma optimization are obtained using the thermionic emission equations:[17,42]

$$I = WR^*T^2 \exp\left(-\frac{q\Phi_{SB}}{kT}\right)\exp\left(\frac{qV_{ds}}{kT}\right), \quad (5)$$

$$\Phi_{SB} = \frac{k}{q}\left[-\frac{\Delta\ln\left(I/T^2\right)}{\Delta T^{-1}}\right], \quad (6)$$

where W, $R^* = q\sqrt{8\pi m^* k^3}/h^2$, T, q, Φ_{SB}, k, and V_{ds} are the channel width, modified Richardson constant, temperature, electron charge, Schottky barrier height, Boltzmann constant, and drain voltage, respectively. Leveraging Eq. (6), we can extract the Schottky barrier heights under the flatband condition at the contacts with/without plasma optimization from the transfer curves measured at different temperatures [Fig. 5(f)]. Both negative values of Φ_{SB} confirm the good contact between the Cr/Au electrode and PdSe₂, and the larger absolute value for Φ_{SB} at $V_{ds} = -1$ V also suggests the plasma-induced p-type doping at the contact with plasma optimization.

The plasma-optimized contact strategy can also be extended to WSe₂ and MoSe₂ FETs (supplementary material Figs. S9 and S10). The insets in supplementary material Figs. S9(a) and S10(a) provide the optical microscopy images of the WSe₂ and MoSe₂ FETs, where the red dashed lines denote the electrodes optimized by plasma, while the blue ones denote the electrodes without. The performance improvement in WSe₂ and MoSe₂ FETs with plasma-optimized contact is proved by their much higher current on/off ratios and carrier mobilities [supplementary material Figs. S9(c), S9(d), S10(c), and S10(d)].

In conclusion, we have developed a plasma-optimized contact strategy for high-performance PdSe₂ nanoflake-based FETs, which is highly compatible with the standard 2D device fabrication process in laboratories. The PdSe₂ FETs with plasma-optimized contact exhibited enhanced field-effect carrier mobilities, higher current on/off ratios, and reduced contact resistance than the pristine PdSe₂ FET fabricated from the same flake. The increased carrier injection efficiency in the optimized contact area can explain the performance improvement.
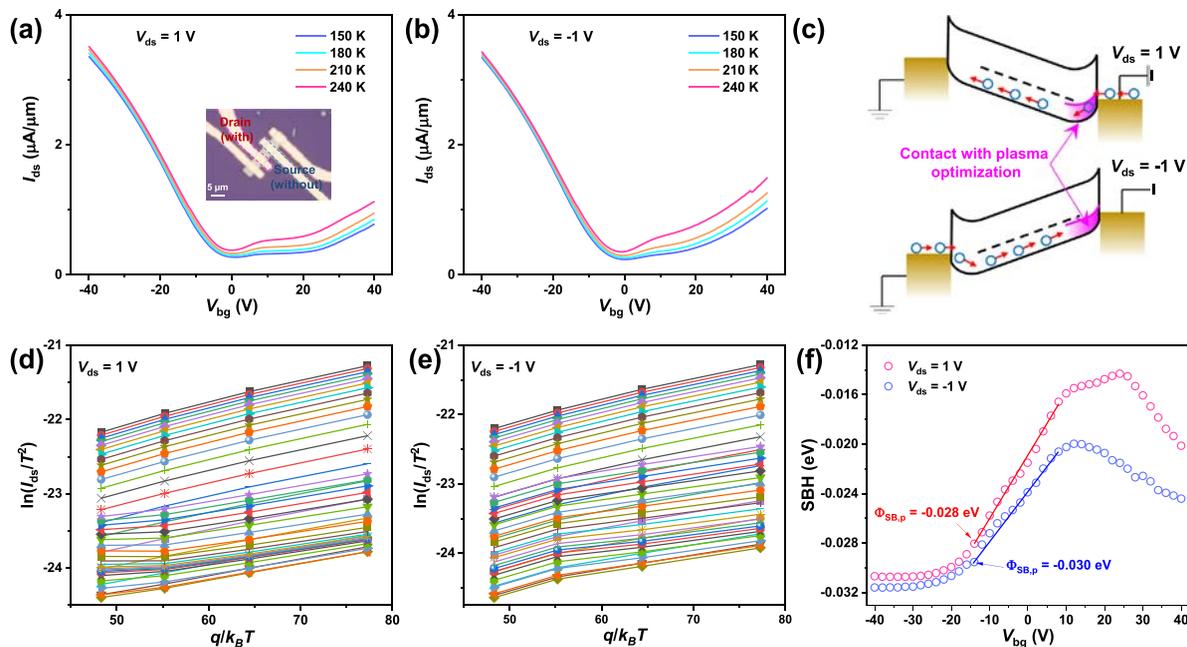
FIG. 5. Low-temperature electrical transport characterization of the PdSe₂ FET with asymmetric contact. Transfer curves measured at different temperatures under the bias of (a) $V_{ds} = 1$ and (b) $V_{ds} = -1$ V. The inset in (a) provides the optical microscopy image of the measured device and depicts the measurement setup. (c) Schematic illustration depicts the band bending under different biases. (d) $\ln(I_{ds}/T^2)$ vs $q/k_B T$ at different gate voltages extracted from (a). (e) $\ln(I_{ds}/T^2)$ vs $q/k_B T$ at different gate voltages extracted from (b). (f) Gate voltage-dependent barrier heights under different biases extracted from (d, e).

In plasma treatment, Se vacancies induced a phase transition from crystalline to amorphous, thus leading to heavy p-type doping, which are corroborated by HRTEM, EDS, and KPFM. In addition to $PdSe_2$, our contact optimization strategy can be further extended to fabricate WSe_2 and $MoSe_2$ FETs with improved electrical performance. This simple but effective strategy may also be applied to prepare high-performance FETs based on other 2D materials.

See the supplementary material for the experimental details of the preparation of $PdSe_2$ FET with/without plasma-optimized contact and performance improvement for WSe_2 and $MoSe_2$ FETs with plasma-optimized contact.

AUTHOR DECLARATIONS
Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Jiajia Zha: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal). **Zhengbao Yang:** Supervision (supporting); Writing – review & editing (supporting). **Ye Chen:** Supervision (supporting); Writing – review & editing (supporting). **Johnny C. Ho:** Project administration (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Chaoliang Tan:** Conceptualization (equal); Funding acquisition (equal); Methodology (equal); Project administration (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Handa Liu:** Conceptualization (supporting); Data curation (supporting); Investigation (supporting); Methodology (supporting); Writing – original draft (supporting). **Huide Wang:** Data curation (supporting); Formal analysis (supporting); Investigation (supporting); Methodology (supporting); Writing – review & editing (supporting). **Siyuan Li:** Data curation (supporting); Investigation (supporting); Methodology (supporting); Writing – review & editing (supporting). **Haoxin Huang:** Data curation (supporting); Formal analysis (supporting); Writing – review & editing (supporting). **Yunpeng Xia:** Data curation (supporting); Formal analysis (supporting); Writing – review & editing (supporting). **Chen Ma:** Data curation (supporting); Formal analysis (supporting); Writing – review & editing (supporting). **Peng Yang:** Data curation (supporting); Formal analysis (supporting); Writing – review & editing (supporting). **Zhuomin Zhang:** Data curation (supporting); Formal analysis (supporting); Writing – review & editing (supporting).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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